7150 Riverwood Dr.
Columbia, MD 21046

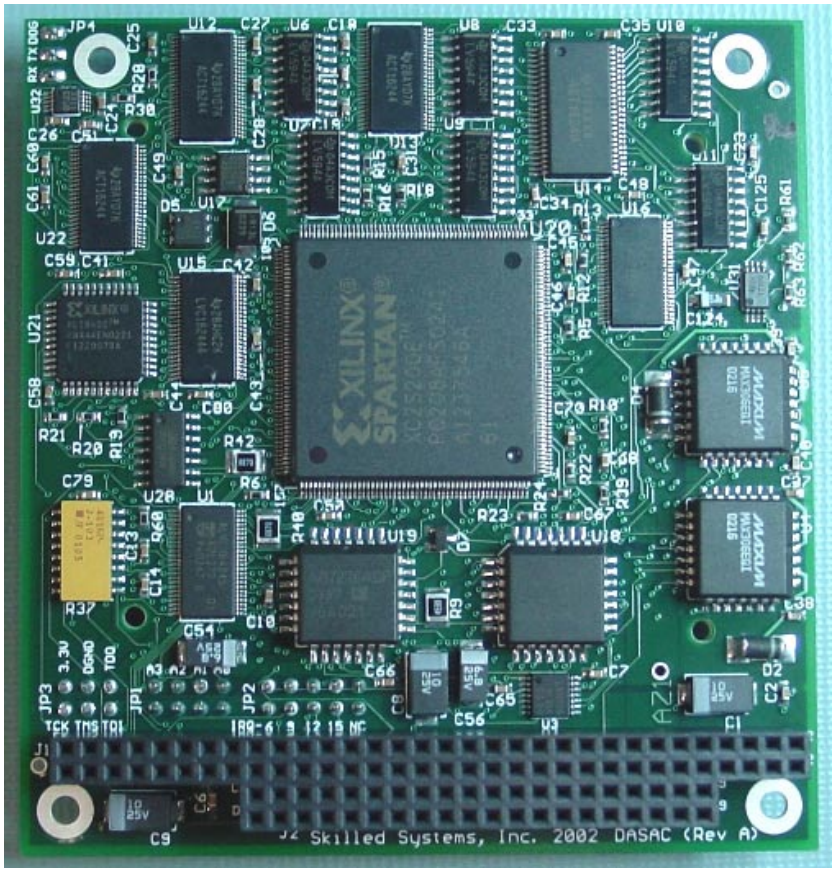
support@skilledsystems.com
www.skilledsystems.com

DASAC

Digital & Analog Sensor & Actuator Controller

User's Manual

V2.00



Skilled Systems, Incorporated
7150 Riverwood Drive
Columbia, Maryland 21046
Tel (410) 290-5662
Fax (410) 290-5664
skilledsystems@skilledsystems.com
www.skilledsystems.com

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

Table of Contents

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

1. Description

The Skilled Systems DASAC is a versatile digital and analog I/O card in a PC/104 format. While suited for sensor and actuator control, the DASAC may be used in any application that would benefit from the numerous user I/O under the control of a host CPU. The DASAC is I/O mapped to the PC/104 bus and is readily controlled from a host processor.

The DASAC features the following I/O types:

- 48 digital outputs (32 non-inverting / 16 inverting)
- 24 digital inputs
- 1 watchdog timer output (based on two gated watchdog timers)
- 1 RS-232 to one-wire interface
- 4 summing amplifier outputs
- 2 16:1 analog muxes (2 sets of 16 analog inputs with 1 analog output)
- 16 analog outputs (with 8-bit resolution)
- 8 digital output pulses

The DASAC is built with industrial components and is specified over the extended temperature range of -40 to 85 ^{o}C.

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

2. Block Diagram

A high-level block diagram is shown in Figure 1.

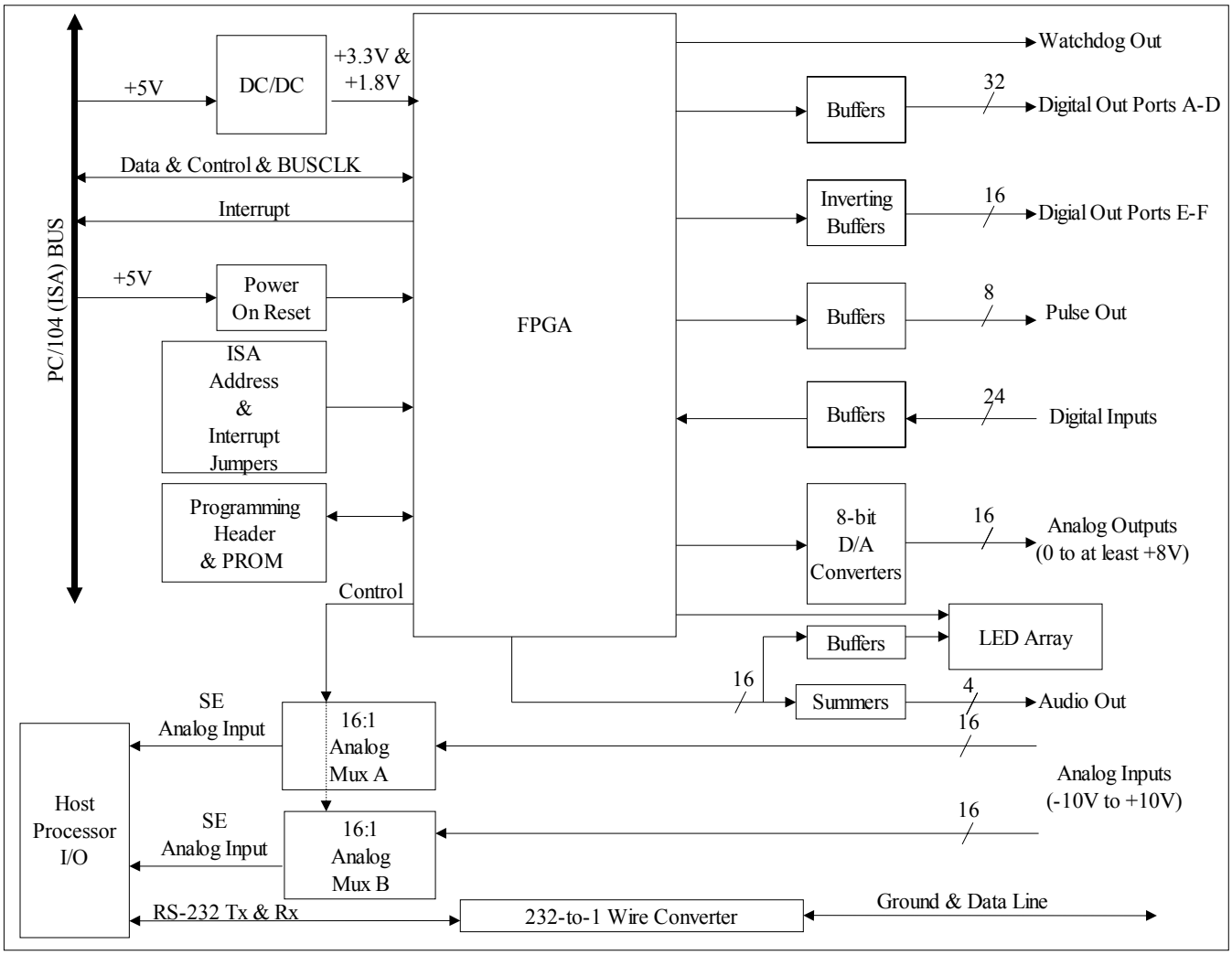


Figure 1: High-Level DASAC Block Diagram

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

3. Board Configuration Drawing

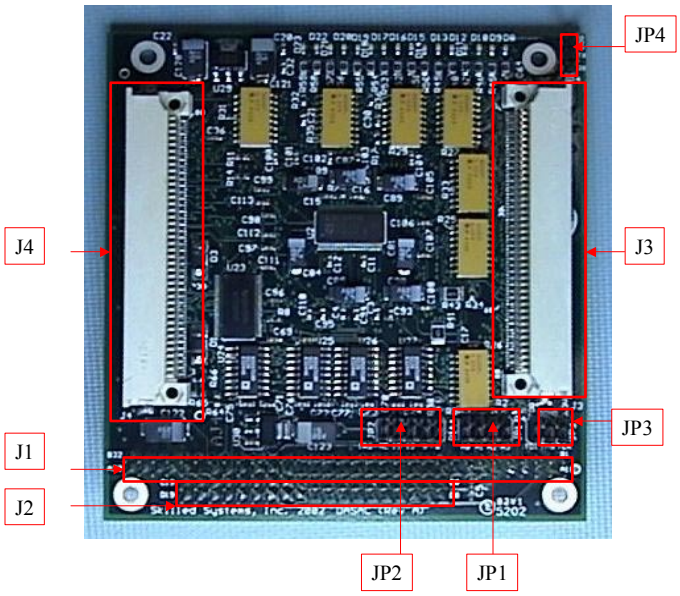


Figure 2 - Jumper Locations

A legend, providing a connector / header function mapping, is shown in Table 1.

J1	PC/104 Bus Header
J2	PC/104 Bus Header
J3	External User Connector (Digital In, Digital Out, Audio Sum Out, Watchdog Out, One Wire)
J4	External User Connector (Analog In, Analog Out, Digital Out, Digital Pulse Out)
JP1	Base Address Header
JP2	Interrupt Level Header
JP3	Test Header (No User Connection)
JP4	Processor Connector (RS-232 TX/RX For One-Wire I/F, Watchdog Out)

Table 1: DASAC Connector / Header Legend

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

4. I/O Header & Connector Pinout and Pin Description

The DASAC utilizes standard PC/104 J1 & J2 bus connectors for signal and power connectivity via the PC/104 bus. Additional information may be found at http://www.pc104.org/.

The DASAC provides two 80-pin Hirose FX2A-80P-0.635SH connectors that serve as the primary interface connectors to the card. These are denoted as J3 and J4.

J3 is primarily a digital I/O connector that provides connections to the 24-bit digital input signals, 16-bit digital output ports B/A and D/C as well as part of inverting port E, audio summation signals, watchdog timer output, and one-wire interface port.

J4 is primarily an analog I/O connector that provides connections to the two 16-bit analog input ports, 16-bit analog output ports, and analog multiplexer outputs. The connector also carries digital signals in providing connections to the two inverting 8-bit digital output ports (E and F) as well as the 8-bit digital pulse output port.

The signal descriptions are shown in Table 2.

Signal Name	Definition
Dig Out B/A [15:0]	Digital output port
Dig Out D/C [15:0]	Digital output port
Dig Out Inv E [1:0]	Digital output (inverted) port (two LSBs only)
Dig In Port #1 [11:0]	Digital input port
Dig In Port #2 [11:0]	Digital input port
#Watchdog Out	Digital watchdog timer output (active low)
Audio Sum Out [4:1]	Analog summer output
232RX Out	RS-232 CPU receive signal
232TX In	RS-232 CPU transmit signal
One Wire	One-wire, bi-directional signal
GND	Ground signal; connected to PC/104 bus ground

Table 2: J3 Signal Descriptions

The signal descriptions are shown in Table 3.

Signal Name	Definition
An In A [15:0]	Analog input channels - A side
An In B [15:0]	Analog input channels - B side
An Mux Out A	Analog multiplexed output of A-side inputs

An Mux Out B	Analog multiplexed output of B-side inputs
An Out [15:0]	Analog signal output port from D/A converter
Dig Out Inv E [7:2]	Digital output (inverted) port (6 MSBs only)
Dig Out Inv F [7:0]	Digital output (inverted) port
Dig Pulse Out [7:0]	Digital output pulse port
GND	Ground signal; connected to PC/104 bus ground

Table 3: J4 Signal Descriptions

The DASAC provides one 8-pin header that is used with shunts to select the PC/104 bus base address. This header is denoted as JP1. The base address selection is discussed in the Board Configuration section of this manual.

1	2	Address Jumper 3
3	4	Address Jumper 2
5	6	Address Jumper 1
7	8	Address Jumper 0

The DASAC provides one 10-pin header that is used with shunts to select the PC/104 bus interrupt level. This header is denoted as JP2. The interrupt level selection is discussed in the Board Configuration section of this manual.

1	2	IRQ6
3	4	IRQ9
5	6	IRQ12
7	8	IRQ15
9	10	[Not Used]

The DASAC provides one 3-pin header connector for connecting specific signals directly to a host processor (or other system card) without utilizing the 80-pin Hirose connector J3. This may be useful depending on a particular system's configuration. This header is denoted as JP4. Note that these signals are the same exact signals that are also connected to J3.

1	232RX Out
2	232TX Out
3	Watchdog Out

The signal descriptions are shown in Table 4.

Signal Name	Definition

232RX Out	RS-232 CPU receive signal
232TX In	RS-232 CPU transmit signal
#Watchdog Out	Digital watchdog timer output (active low)

Table 4: JP4 Header Signal Descriptions

5. Board Configuration

Each board in the PC/104 system must have a different base address. The DASAC's base address is set with four address jumper pairs marked "A3", "A2", "A1", and "A0" on header JP1. JP1 is located near the bottom of the board near the PC/104 connectors. The jumper configurations and corresponding base addresses are listed in Table 5. Note that "Off" indicates that no shunt in present on the particular jumper, while "On" indicates that a shunt is installed on the particular jumper.

Base Address (Hex)	Address Jumper 3	Address Jumper 2	Address Jumper 1	Address Jumper 0
100	Off	On	On	On
140	On	Off	On	Off
180	On	Off	Off	On
1C0	On	Off	Off	Off
200	Off	On	On	On
240	Off	On	On	Off
280	Off	On	Off	On
2C0	Off	On	Off	Off
300	Off	Off	On	On
340	Off	Off	On	Off
380	Off	Off	Off	On
3C0	Off	Off	Off	Off

Table 5: DASAC Base Address Configuration

The DASAC can generate a processor interrupt based on a periodic counter value as set by the user. The user may set the interrupt pin (level) that is used in the system via a shunt placed on JP2. Interrupt Request (IRQ) levels 6, 9, 12, and 15 are available and are indicated on the circuit board. The DASAC does not support interrupt sharing. Note that two watchdog timers in the DASAC may be used to generate a *separate* watchdog timer output signal (i.e. not the bus interrupt signal) to a host processor.

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

6. Command & Register Map

The DASAC occupies 29 16-bit words in the PC/104 system I/O space. All command execution and register accesses (reads and writes) are invoked by 16-bit software reads and writes to the particular I/O address. In the event where less than 16 data bits are required to be written or read, the unused bits can be considered as "don't care" values. Software may use any value when writing the "don't care" bits and should discard the "don't care" bits when reading. The command and register map is shown in Table 6.

The DASAC utilizes the PC/104 SYSCLK signal as the main clock in executing commands and setting register values. The frequency of SYSCLK may vary among processor cards and manufacturers. It is essential that the user verify the SYSCLK frequency in the target system.

Base + (Hex)	Write Function	Read Function
0	Write Interrupt & Control Register	Read Board Status Register
2	Software Reset Card	Read Digital Inputs - Digin Port 1
4	Pet Watchdog Timer A	Read Digital Inputs – Digin Port 2
6	Select Analog Input A and B	Read Audio & LED Output Select Reg#1
8	Write To Digital Output Port B/A	Read Audio & LED Output Select Reg#2
A	*[Reserved]*	*[Reserved]*
C	Write To Digital Output Port D/C	*[Reserved]*
E	*[Reserved]*	*[Reserved]*
10	Write To Digital Output Port E	*[Reserved]*
12	Write To Digital Output Port F	*[Reserved]*
14	Write Digital Output Port Enable	*[Reserved]*
16	Write Output Pulse Configuration Register	*[Reserved]*
18	Write Output Pulse Width & Frequency Register	*[Reserved]*
1A	Assert Output Pulse #n	*[Reserved]*
1C	Write To Audio & LED Output Select Register #1	*[Reserved]*
1E	Write To Audio & LED Output Select Register #2	*[Reserved]*
20	Write To Audio & LED Output Select Register #3	*[Reserved]*
22	Write To Audio & LED Output Select Register #4	*[Reserved]*
24	Write To Enable / Disable LED Indicators	*[Reserved]*
26	Write To D/A Select Register	*[Reserved]*
28	Write D/A Data	*[Reserved]*
2A	Write To Periodic Interrupt Interval (Lower Bits)	*[Reserved]*
2C	Write To Periodic Interrupt Interval (Upper Bits)	*[Reserved]*
2E	Pet Watchdog Timer B	*[Reserved]*
30	*[Reserved]*	*[Reserved]*
32	Write To Watchdog Disable Register #1	*[Reserved]*
34	*[Reserved]*	*[Reserved]*
36	*[Reserved]*	*[Reserved]*
38	Write To Watchdog Disable Register #2	*[Reserved]*

Table 6: DASAC Command & Register Map

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

7. I/O Register Definitions

Write Commands

Base + 0 Write Write Interrupt & Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	PDCNTEN	PDMSK	INTEN

Definitions:
INTEN Enables interrupt driver to PC/104 bus (1 = enabled, 0 = disabled)
PDMSK Logical mask for periodic interrupt (1 = enabled, 0 = disabled)
PDCCNTEN Periodic counter enable (1 = counting, 0 = not counting).

Default Value: 0x0

Base + 2 Write Software Reset Card

Writing to Base + 2 causes all clocked elements on the DASAC card to be reset to their default conditions. The value written does not matter.

Base + 4 Write Pet Watchdog Timer #1

Writing to Base + 4 causes the watchdog timer #1 to be restarted such that the watchdog timer does not expire. The value written does not matter. Depending on settings made via commands Base + 32 and Base + 38, the expiration of the watchdog timer may result in a low-going pulse output (one SYSCLK wide) and a set bit in the board status register.

Watchdog timer #1, when enabled, is a free-running 16-bit counter. When the terminal value of 0xFFFF is reached, the counter rolls over to 0x0000, and the watchdog signal is asserted.

The watchdog #1 timeout = (65535 x SYSCLK period).

Base + 6 Write Write Analog Input Select Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	BSEL3	BSEL2	BSEL1	BSEL0	ASEL3	ASEL2	ASEL1	ASEL0

Definitions:
ASEL Analog Input A[15:0] multiplexer selection value
BSEL Analog Input B[15:0] multiplexer selection value

Writing to ASEL causes the DASAC to output one of sixteen analog inputs (An In A) to be output on the An Mux Out A signal.

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

Writing to BSEL causes the DASAC to output one of sixteen analog inputs (An In B) to be output on the An Mux Out B signal.

Default Value: 0x00

Base + 8 Write Write To Digital Output Port B/A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B/A15	B/A14	B/A13	B/A12	B/A11	B/A10	B/A9	B/A8	B/A7	B/A6	B/A5	B/A4	B/A3	B/A2	B/A1	B/A0

Definitions:
B/A[15:0] Sixteen bit digital output port B/A

The value written to this port will be output on signals Dig Out B/A[15:0] if enabled (Base + 14).

Default Value: 0x0000

Base + C Write Write To Digital Output Port D/C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D/C15	D/C14	D/C13	D/C12	D/C11	D/C10	D/C9	D/C8	D/C7	D/C6	D/C5	D/C4	D/C3	D/C2	D/C1	D/C0

Definitions:
D/C[15:0] Sixteen bit digital output port D/C

The value written to this port will be output on signals Dig Out D/C[15:0] if enabled (Base + 14).

Default Value: 0x0000

Base + 10 Write Write To Digital Output Inverted Port E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	E7	E6	E5	E4	E3	E2	E1	E0

Definitions:
E[7:0] Eight bit digital output inverted port E

The complement of the value written to this port will be output on signals Dig Out E[7:0] if enabled (Base + 14).

Default Value: 0xFF

Base + 12 Write Write To Digital Output Inverted Port F

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	F7	F6	F5	F4	F3	F2	F1	F0

Definitions:
F[7:0] Eight bit digital output inverted port F

The complement of the value written to this port will be output on signals Dig Out F[7:0] if enabled (Base + 14).

Default Value: 0xFF

Base + 14 Write Write To Digital Output Port Enable

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DIGOUTEN

Definitions:
DIGOUTEN One bit digital output port enable (1 = All digital output ports enabled, 0 = disabled)

When digital outputs B/A and D/C are disabled, a 10k pulldown resistor on each output keeps each signal at 0V.

When digital outputs E and F are disabled, a 10k pullup resistor on each output keeps each signal at +5V.

Default Value: 0x0

Base + 16 Write Write To Output Pulse Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RPT7	RPT6	RPT5	RPT4	RPT3	RPT2	RPT1	RPT0	POL7	POL6	POL5	POL4	POL3	POL2	POL1	POL0

Definitions:
POL[7:0] Active high or low selection for Dig Pulse Out [7:0] (one bit for each pulse)
1 = Active High, 0 = Active Low

RPT[7:0] Repetitive or single shot pulse for Dig Pulse Out [7:0] (one bit for each pulse)
1 = Repetitive, 0 = Single Shot

The results of the repetition and polarity settings for each of the eight pulses are observed on the Dig Pulse Out [7:0] signals as controlled by the Base +18 and Base +1A commands.

Note that a pulse train caused by a pulse being put in repetitive mod may be stopped by setting the repetition setting to 0 (single shot) at any time.

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

Default Value: 0x00FF

Base + 18 Write Write To Pulse Width & Frequency Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INAC7	INAC6	INAC5	INAC4	INAC3	INAC2	INAC1	INAC0	WID7	WID6	WID5	WID4	WID3	WID2	WID1	WID0

Definitions:

WID[7:0] Pulse width for all Dig Pulse Out [7:0] signals
Pulse width = (value x 1024 x SYSCLK period)

INAC[7:0] Pulse inactive time for all Dig Pulse Out [7:0] signals
Pulse inactive time = (value x 4096 x SYSCLK period)

Note that pulse frequency (in repetitive mode) = 1 / (Pulse inactive time + Pulse Width).

The results of the inactive and width settings are observed on the Dig Pulse Out [7:0] signals as controlled by the Base +16 and Base +1A commands.

Default Value: 0x995C

Base + 1A Write Assert Output Pulse #n

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	PEN	AOP7	AOP6	AOP5	AOP4	AOP3	AOP2	AOP1	AOP0

Definitions:

AOP[7:0] Writing to any (or any combination) of these bit locations will cause the particular pulse to be asserted. These register bits are self-clearing. If the given pulse output has been set (via Base +16) to single shot, one pulse will be output. However, if the given pulse has been set to repetitive mode, then pulse outputs will occur at a rate as set in Base +18. A repetitive pulse train may be stopped at any time by designating that pulse a single shot.

PEN Master output pulse enable (1 = Enable pulse outputs, 0 = Disable pulse outputs). When digital output pulses are disabled, a 10k pulldown resistor on each pulse output keeps each signal at 0V.

Default Value: 0x00

Base + 1C Write Write To Audio & LED Output Select Register #1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

BIT3-3	BIT3-2	BIT3-1	BIT3-0	BIT2-3	BIT2-2	BIT2-1	BIT2-0	BIT1-3	BIT1-2	BIT1-1	BIT1-0	BIT0-3	BIT0-2	BIT0-1	BIT0-0

Definitions:
BITx-[3:0] Select bits for LED & audio summer multiplexer outputs

BIT0-[3:0] to BIT15-[3:0] are select bits for LEDs D8 to D23 (as marked on the DASAC card).

Analog Summer Output #1 is comprised of multiplexed outputs [3:0].

Refer to Appendix A for the multiplexing options.

Default Value: 0x00

Base + 1E Write Write To Audio & LED Output Select Register #2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT7-3	BIT7-2	BIT7-1	BIT7-0	BIT6-3	BIT2-2	BIT6-1	BIT6-0	BIT5-3	BIT5-2	BIT5-1	BIT5-0	BIT4-3	BIT4-2	BIT4-1	BIT4-0

Definitions:
BITx-[3:0] Select bits for LED & audio summer multiplexer outputs

BIT0-[3:0] to BIT15-[3:0] are select bits for LEDs D8 to D23 (as marked on the DASAC card).

Analog Summer Output #2 is comprised of multiplexed outputs [7:4].

Refer to Appendix A for the multiplexing options.

Default Value: 0x00

Base + 20 Write Write To Audio & LED Output Select Register #3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT11-3	BIT11-2	BIT11-1	BIT11-0	BIT10-3	BIT10-2	BIT10-1	BIT10-0	BIT9-3	BIT9-2	BIT9-1	BIT9-0	BIT8-3	BIT8-2	BIT8-1	BIT8-0

Definitions:
BITx-[3:0] Select bits for LED & audio summer multiplexer outputs

BIT0-[3:0] to BIT15-[3:0] are select bits for LEDs D8 to D23 (as marked on the DASAC card).

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

Analog Summer Output #3 is comprised of multiplexed outputs [11:8].

Refer to Appendix A for the multiplexing options.

Default Value: 0x00

Base + 22 Write Write To Audio & LED Output Select Register #4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT15-3	BIT15-2	BIT15-1	BIT15-0	BIT14-3	BIT14-2	BIT14-1	BIT14-0	BIT13-3	BIT13-2	BIT13-1	BIT13-0	BIT12-3	BIT12-2	BIT12-1	BIT12-0

Definitions:

BITx-[3:0] Select bits for LED & audio summer multiplexer outputs

BIT0-[3:0] to BIT15-[3:0] are select bits for LEDs D8 to D23 (as marked on the DASAC card).

Analog Summer Output #3 is comprised of multiplexed outputs [15:12].

Refer to Appendix A for the multiplexing options.

Default Value: 0x00

Base + 24 Write Write To Enable / Disable LED Indicators

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LEDST	X	X	X	X	X	X	X	X	X	X	X	X	X	X	LEDEN

Definitions:

LEDEN Global LED enable (1 = Enabled, 0 = Disabled).
Note that if the LEDST bit is set, the LED blink pattern will be displayed regardless of the LEDEN bit's setting.

LEDST Writing a logic 1 to this bit causes the LEDs to blink per a pre-defined pattern. This bit position is self-clearing.

Default Value: 0x00

Base + 26 Write Write To D/A Select Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

X	X	X	X	X	X	X	X	X	X	X	ANOUTEN	ANSEL3	ANSEL2	ANSEL1	ANSEL0

Definitions:

ANSEL[3:0] Select lines for choosing the D/A converter.
D/A converter outputs correspond to analog outputs (An Out [15:0]).
This value is written prior to writing data to a particular D/A converter (Base + 28)

ANOUTEN Global analog output enable (1 = Enabled, 0 = Disabled).
When analog outputs are disabled, a 10k pulldown resistor on each analog output keeps each signal at 0V.

Default Value: 0x00

Base + 28 Write Write D/A Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	DAD7	DAD6	DAD5	DAD4	DAD3	DAD2	DAD1	DAD0

Definitions:

DAD[7:0] 8-bit D/A converter value.
The value written to DAD[7:0] is automatically written to the D/A converter as currently selected (Base + 26).

The voltage that appears on the selected An Out[15:0] line may be computed as follows:

D/A converter voltage = (DAD[7:0] Value / 256) x 8.192V.

Default Value: 0x00

Base + 2A Write Write Periodic Interrupt Interval Lower Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	PIN9	PIN8	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0

Definitions:

PIN[15:0] Lower 16-bits of a user-defined 22-bit periodic interrupt interval.
This value is set in conjunction with the upper 6 bits (Base +2C).
The periodic counter should be disabled (stopped) when setting these values (Base + 0).

These 22 bits are the upper 22 bits of a 23-bit counter with the LSB fixed at 1.

When enabled, the 23-bit periodic counter counts down to zero, at which point, the counter rolls over to the original value (user defined 22-bit value & “1”) and an

interrupt pulse is generated. A bit in the status register is also set (which may be useful for polling if the bus interrupt is disabled).

Default Value: 0xF41

Base + 2C Write Write Periodic Interrupt Interval Upper Bits

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	PIN21	PIN20	PIN19	PIN18	PIN17	PIN16

Definitions:

PIN[21:16] Upper 6-bits of a user-defined 22-bit periodic interrupt interval.
This value is set in conjunction with the lower 16 bits (Base +2A).
The periodic counter should be disabled (stopped) when setting these values (Base + 0).

These 22 bits are the upper 22 bits of a 23-bit counter with the LSB fixed at 1.

When enabled, the 23-bit periodic counter counts down to zero, at which point, the counter rolls over to the original value (user defined 22-bit value & “1”) and an interrupt pulse is generated. A bit in the status register is also set (which may be useful for polling if the bus interrupt is disabled).

Default Value: 0x00

Base + 2E Write Pet Watchdog Timer #2

Writing to Base + 4 causes the watchdog timer #2 to be restarted such that the watchdog timer does not expire. The value written does not matter. Depending on settings made via commands Base + 32 and Base + 38, the expiration of the watchdog timer may result in a low-going pulse output (one SYSCLK wide) and a set bit in the board status register.

Watchdog timer #2, when enabled, is a free-running 24-bit counter. When the terminal value of 0xFFFFFF is reached, the counter rolls over to 0x000000, and the watchdog signal is asserted.

The watchdog #2 timeout = (16777215 x SYSCLK period).

Base + 32 Write Write To Watchdog Disable Register #1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	WD2EN_1	WD1EN_1

Definitions:

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

WD1EN_1 Watchdog timer #1 enable (1 = disabled; 0 = enabled).
In order for watchdog timer #1 to be disabled, the WD1EN_2 bit in the Watchdog Disable Register #2 (Base + 38) must also be set to a logic 1.

WD2EN_1 Watchdog timer #2 enable (1 = enabled; 0 = disabled).
In order for watchdog timer #2 to be disabled, the WD2EN_2 bit in the Watchdog Disable Register #2 (Base + 38) must also be set to a logic 1.

Default Value: 0x00

Base + 38 Write Write To Watchdog Disable Register #1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	WD2EN_2	WD1EN_2

Definitions:

WD1EN_2 Watchdog timer #1 enable (1 = disabled; 0 = enabled).
In order for watchdog timer #1 to be disabled, the WD1EN_1 bit in the Watchdog Disable Register #1 (Base + 32) must also be set to a logic 1.

WD2EN_2 Watchdog timer #2 enable (1 = enabled; 0 = disabled).
In order for watchdog timer #2 to be disabled, the WD2EN_1 bit in the Watchdog Disable Register #2 (Base + 38) must also be set to a logic 1.

Default Value: 0x00

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

Read Commands

Base + 0 Read Read Board Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0	X	X	X	X	X	PDINT	WD2	WD1

Definitions:

WD1	Watchdog timer #1 expired
WD2	Watchdog timer #2 expired
PDINT	Interrupt due to periodic interrupt
VN[7:0]	FPGA Version #

Note that WD1, WD2, and PDINT are self-clearing bits upon reading from this register.

Default Value: 0x6000
(At the time of writing this manual, the FPGA version # = 6)

Base + 2 Read Read Digital Inputs – Digin Port 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D1-11	D1-10	D1-9	D1-8	D1-7	D1-6	D1-5	D1-4	D1-3	D1-2	D1-1	D1-0

Definitions:

D1-[11:0] Digin [11:0] Port #1

The read value reflects the state of the DIGIN Port #1 signals at the time that the read occurs. Care should be taken when DIGIN signals are toggling, as it is possible to violate timing margins during transitional times.

Each digital input signal has a 1k pulldown resistor to prevent inputs from floating when no digital input signal is connected.

Default Value: 0x000

Base + 4 Read Read Digital Inputs – Digin Port 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	D2-11	D2-10	D2-9	D2-8	D2-7	D2-6	D2-5	D2-4	D2-3	D2-2	D2-1	D2-0

Definitions:

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

D2-[11:0] Digin [11:0] Port #2

The read value reflects the state of the DIGIN Port #2 signals at the time that the read occurs. Care should be taken when DIGIN signals are toggling, as it is possible to violate timing margins during transitional times.

Each digital input signal has a 1k pulldown resistor to prevent inputs from floating when no digital input signal is connected.

Default Value: 0x000

Base + 6 Read Read Audio # LED Output Select Register #1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT3-3	BIT3-2	BIT3-1	BIT3-0	BIT2-3	BIT2-2	BIT2-1	BIT2-0	BIT1-3	BIT1-2	BIT1-1	BIT1-0	BIT0-3	BIT0-2	BIT0-1	BIT0-0

Definitions:
BITx-[3:0] Select bits for LED & audio summer multiplexer outputs

The readback function is provided for test purposes only.

Default Value: 0x00

Base + 8 Read Read Audio # LED Output Select Register #2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT7-3	BIT7-2	BIT7-1	BIT7-0	BIT6-3	BIT2-2	BIT6-1	BIT6-0	BIT5-3	BIT5-2	BIT5-1	BIT5-0	BIT4-3	BIT4-2	BIT4-1	BIT4-0

Definitions:
BITx-[3:0] Select bits for LED & audio summer multiplexer outputs

The readback function is provided for test purposes only.

Default Value: 0x00

Default Value: 0x00

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

8. One-Wire Interface

An RS-232 -to- one-wire interface is provided on the DASAC card. This allows a host PC, via its serial port, the ability to send commands through the DASAC card and onto the one-wire output signal. This message may then be received by other downstream devices. Likewise, the DASAC can receive commands via the one-wire interface and transmit this data to the serial port of the host PC.

The one-wire interface is implemented with a DS2480B Serial 1-Wire Line Driver chip. More information may be found at www.maxim-ic.com.

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

9. Specifications

Analog Inputs

Analog Input Range	-12V to +12V

Analog Outputs

Analog Mux Output Range	-12V to +12V
D/A Converter Resolution	8-bits
D/A Converter Output	0V to 8.16V (Vout = Dn x 8.192V, where Dn = 0 to 255/256) into 2k load
Analog Summer Output	-9.8V to +9.5V into 10k load; Up to +/-35 mA.

Digital I/O

All inputs (excluding RS-232)	TTL & CMOS compatible
Watchdog Timer Output	Logic 0: 0V min, 0.55V max; Logic 1: 2V min (at 20mA load), +3.3V max
Digital Output Ports A-F	Logic 0: 0V min, 0.44V max; Logic 1: 4V min (at 24mA load), +5V max
Pulse Outputs	Logic 0: 0V min, 0.55V max; Logic 1: 2.2V min (at 24mA load), +5V max

General

Power Supply	+5V +/- 25%
Current Consumption	100m amps
Operating Temperature	-40 to 85 ^{o}C (Industrial Temperature Range)
Interface	PC/104 (ISA) 16-Bit I/O Mapped

7150 Riverwood Dr.
Columbia, MD 21046

support@skilledsystems.com
www.skilledsystems.com

10. Appendix A

Audio / LED Multiplexing										
Audio/LED Output Signal	**Available Signals**									**Register & Select Bits**
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**		
bit0	a0	a1	c0	c1	e0	f1	"1"	"0"		Reg 1, [3:0]
bit1	a2	a3	c2	c3	e1	f3	"1"	"0"		Reg 1, [7:4]
bit2	a4	a5	c4	c5	e2	f5	"1"	"0"		Reg 1, [11:8]
bit3	a6	a7	c6	c7	e3	f7	"1"	"0"		Reg 1, [15:12]
bit4	b1	b0	d1	d0	e4	f0	"1"	"0"		Reg 2, [3:0]
bit5	b3	b2	d3	d2	e5	f2	"1"	"0"		Reg 2, [7:4]
bit6	b5	b4	d5	d4	e6	f4	"1"	"0"		Reg 2, [11:8]
bit7	b7	b6	d7	d6	e7	f6	"1"	"0"		Reg 2, [15:12]
bit8	a0	a1	c0	c1	e0	f1	"1"	"0"		Reg 3, [3:0]
bit9	a2	a3	c2	c3	e1	f3	"1"	"0"		Reg 3, [7:4]
bit10	a4	a5	c4	c5	e2	f5	"1"	"0"		Reg 3, [11:8]
bit11	a6	a7	c6	c7	e3	f7	"1"	"0"		Reg 3, [15:12]
bit12	b1	b0	d1	d0	e4	f0	"1"	"0"		Reg 4, [3:0]
bit13	in0	in6	in13	in18	in1	in7	"1"	"0"		Reg 4, [7:4]
bit14	in2	in9	in15	in20	in3	in8	"1"	"0"		Reg 4, [11:8]
bit15	in4	in11	in16	in22	in5	in10	"1"	"0"		Reg 4, [15:12]